

Fig.1

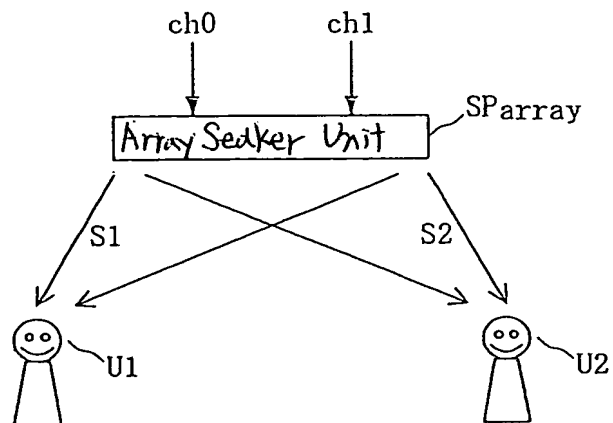


Fig.2

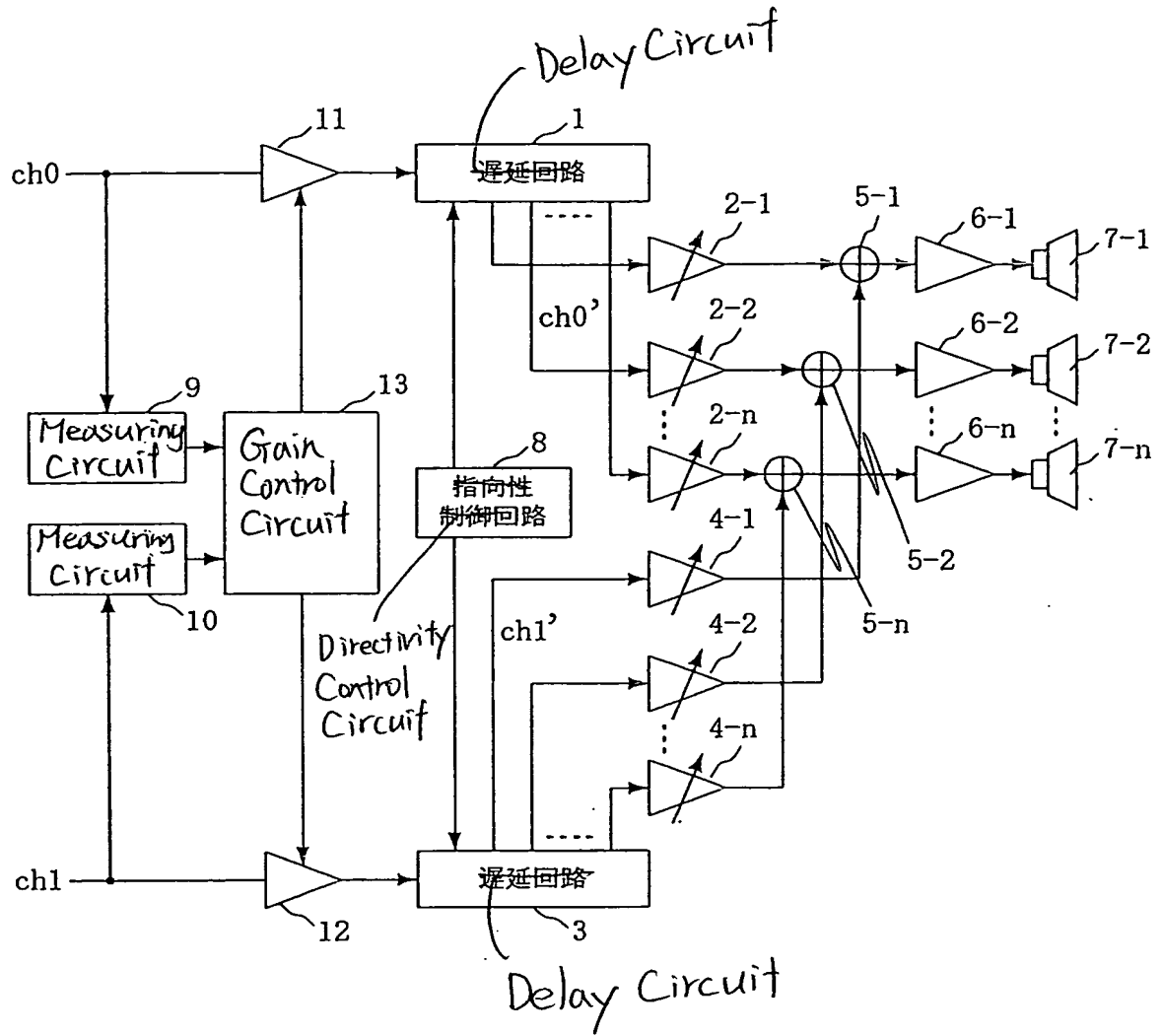


図3
Fig 3

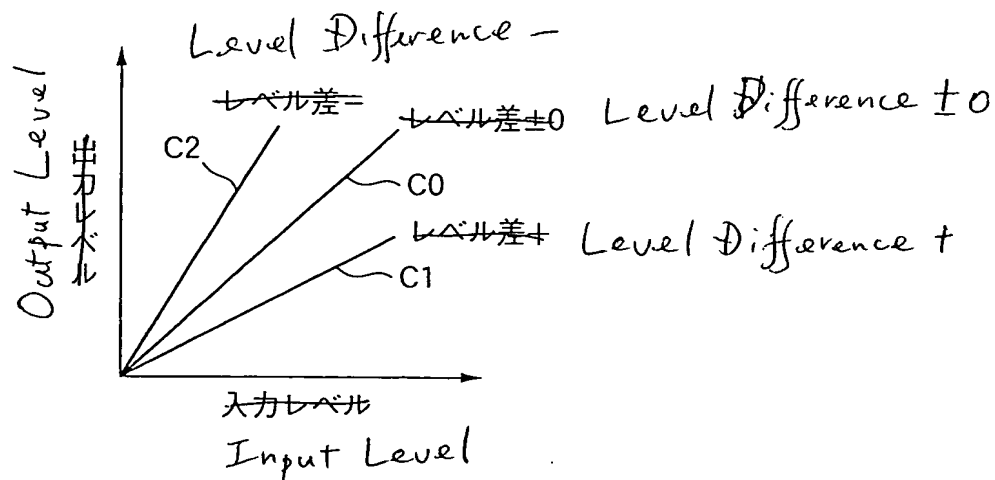


図4
Fig 4

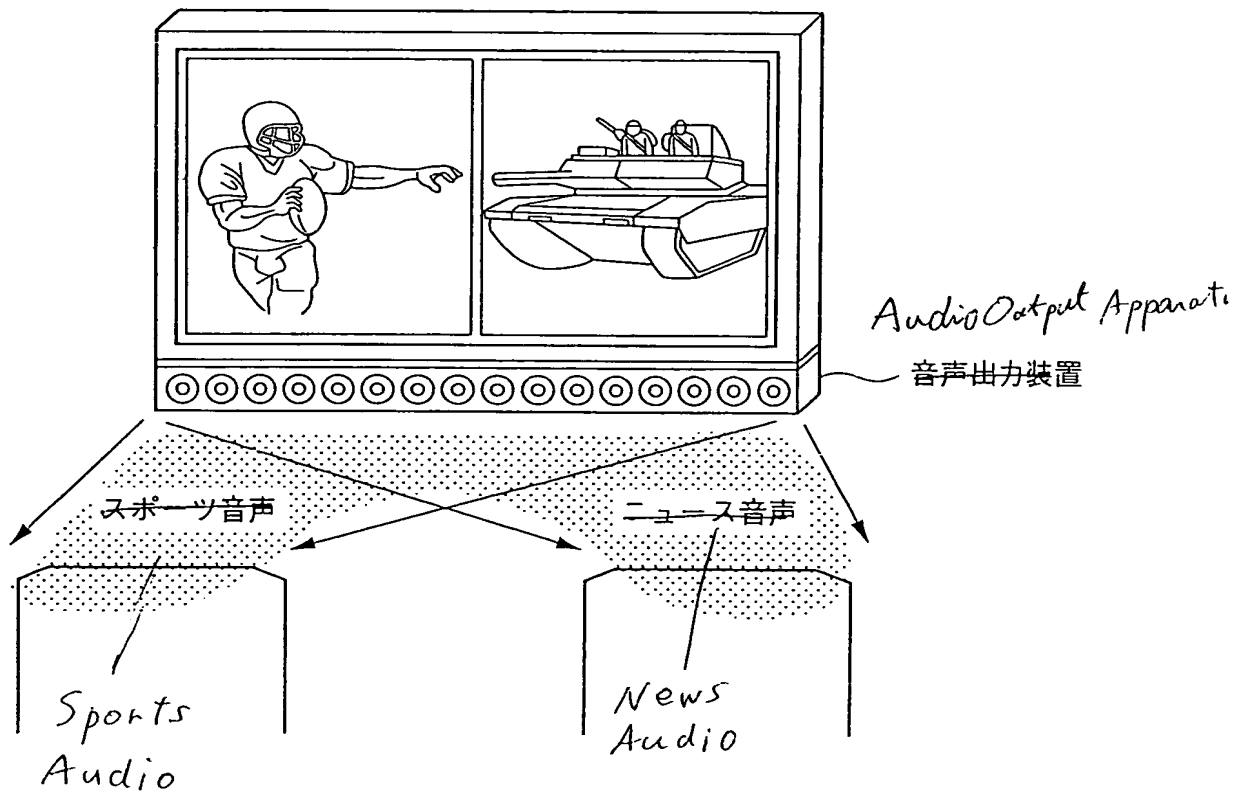


図5
Fig 5

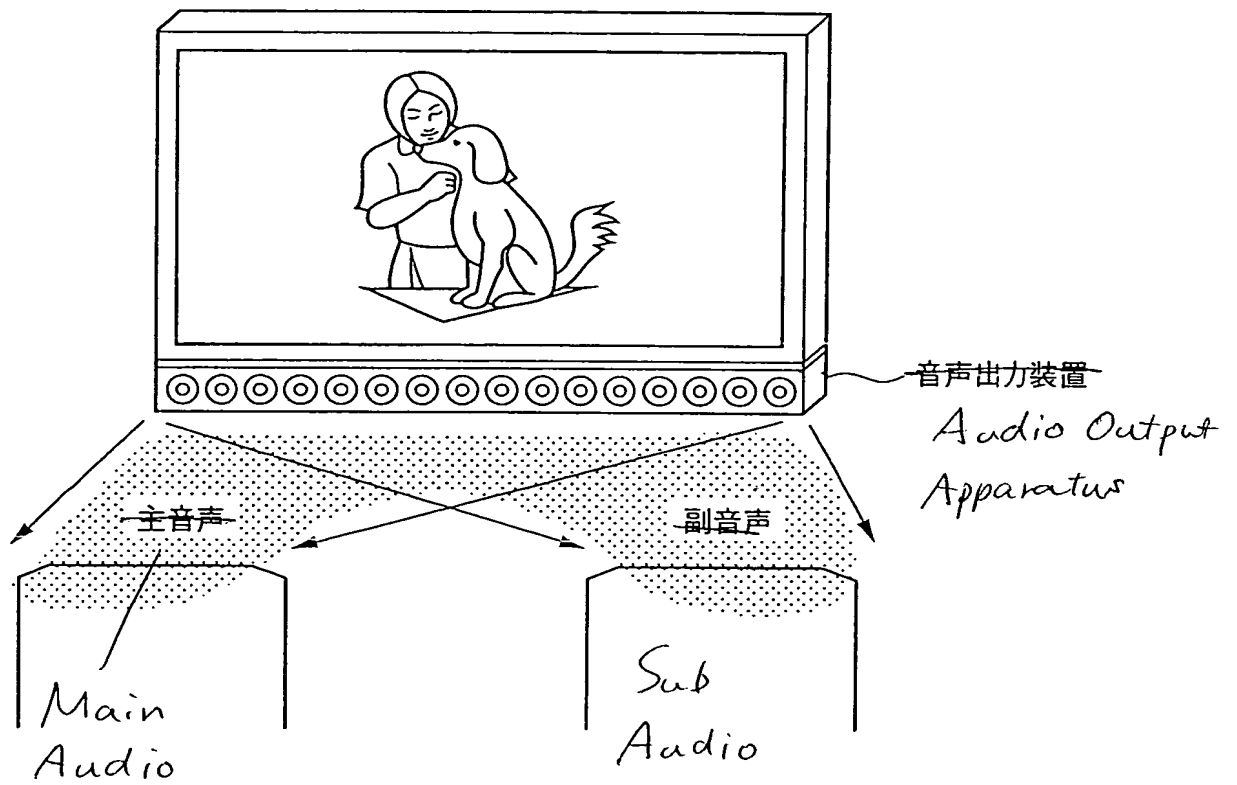
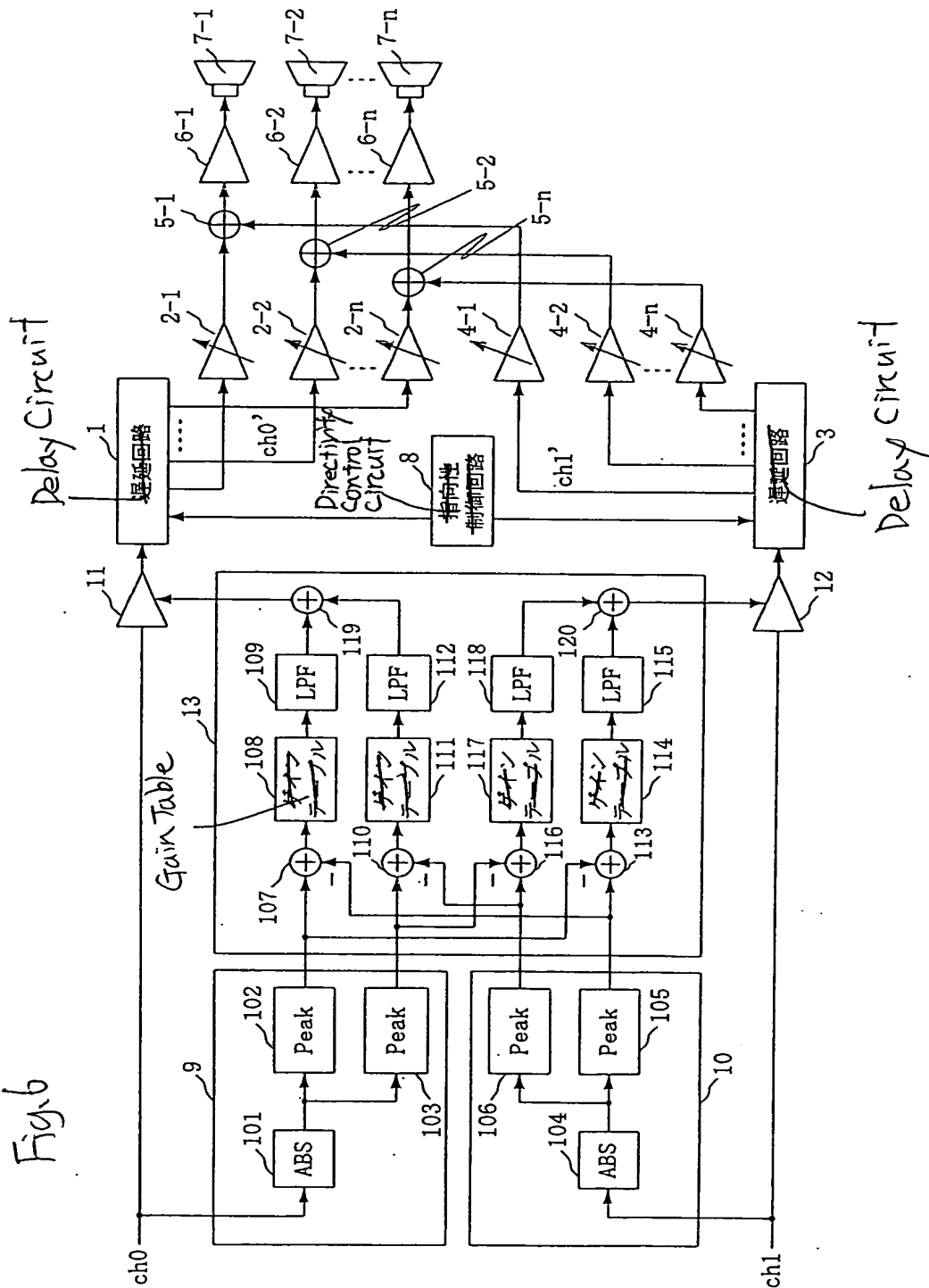


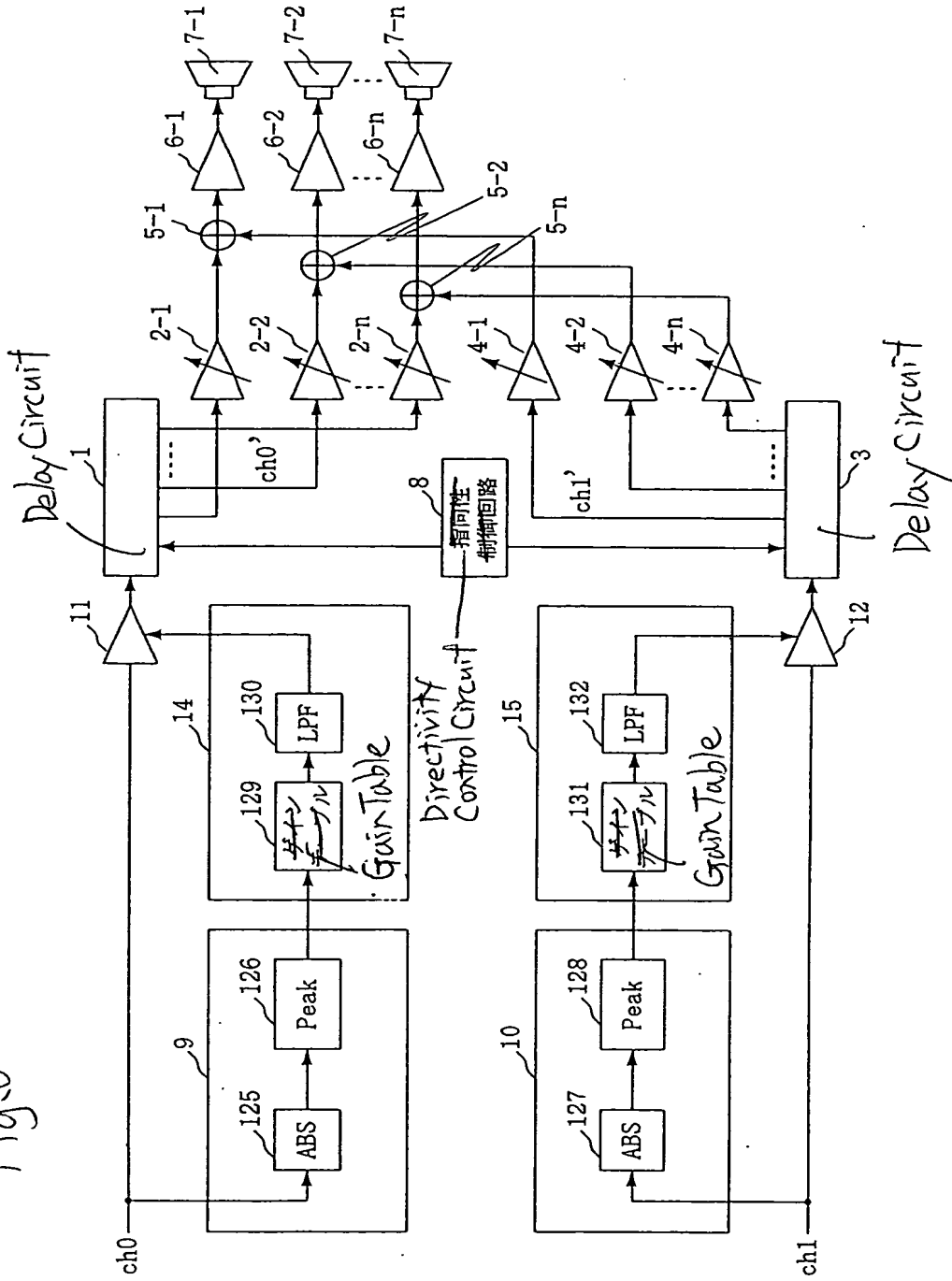
Fig.6



Delay Circuit



Fig.8



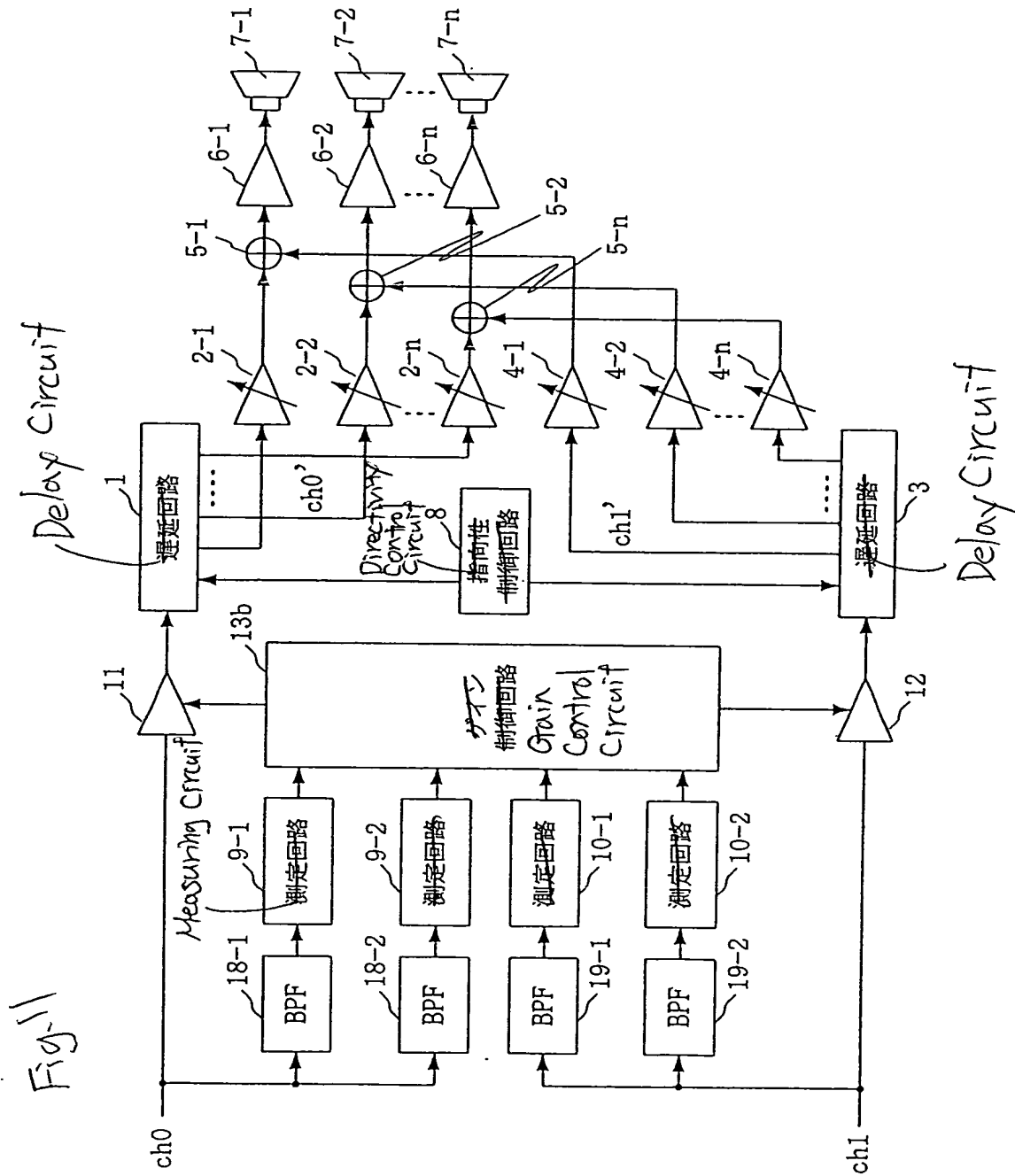


Fig. 12

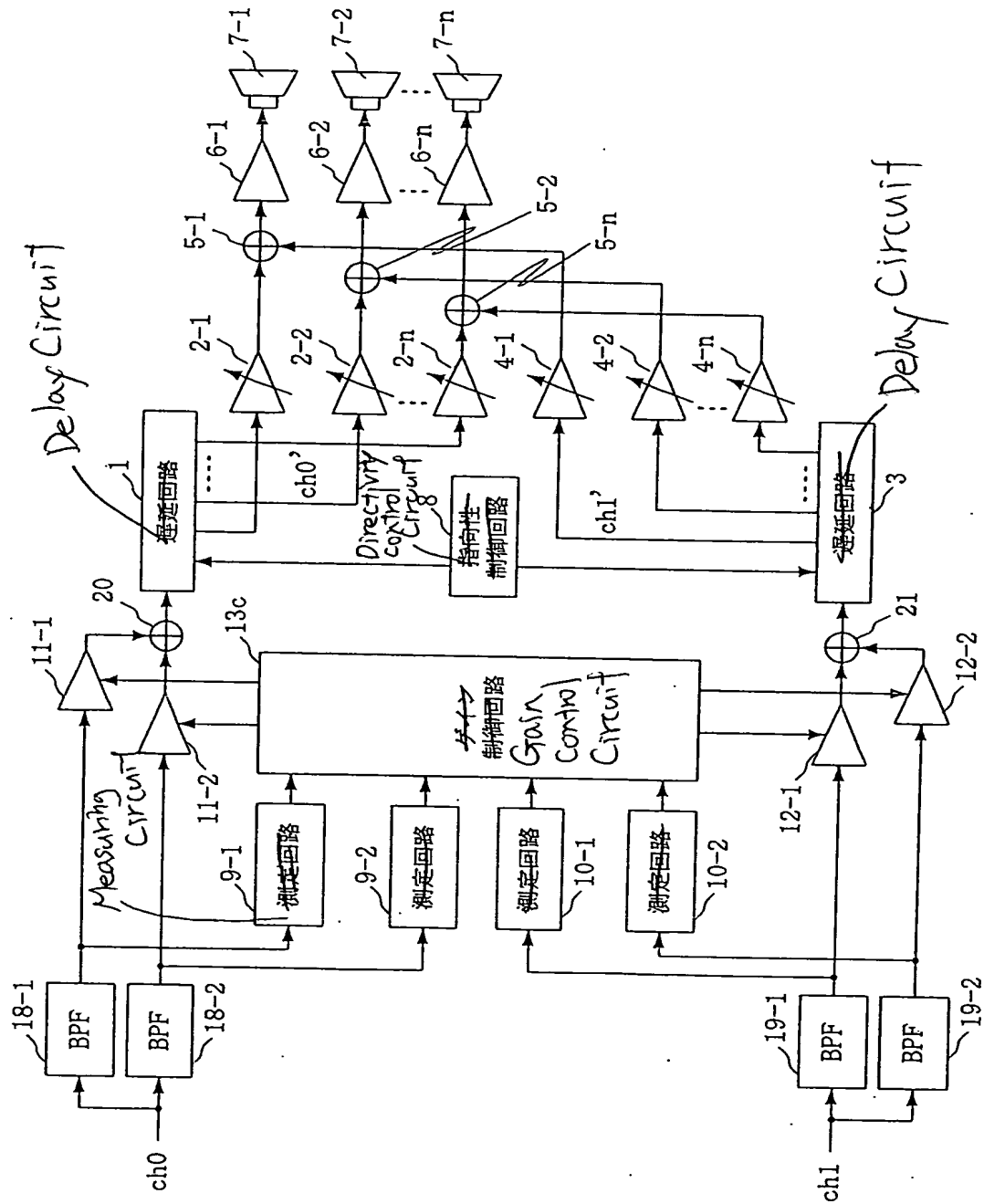


Fig. 13

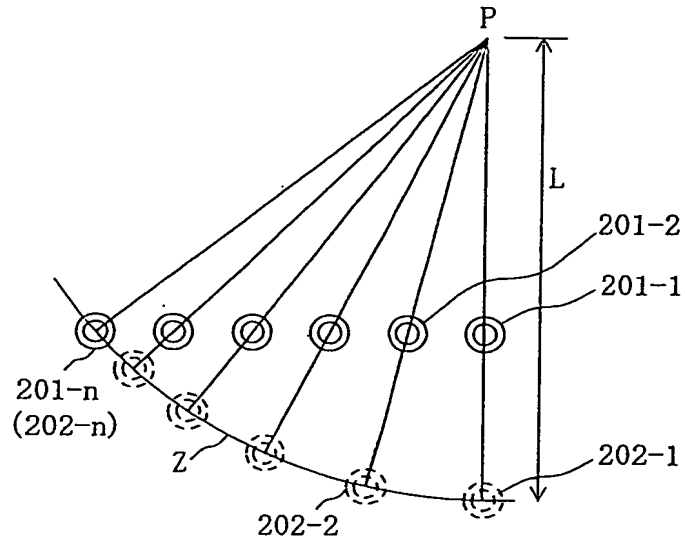


Fig. 14

